IEEE Journal of Emerging and Selected Topics in Power Electronics

Simple and Effective Adaptive Deadtime Strategies for LLC Resonant Converter: Analysis, Design, and Implementation

Yuqi Wei, *Student Member, IEEE*, Quanming Luo, *Member, IEEE*, Zhiqing Wang, and H. Alan Mantooth, *Fellow, IEEE*

***Abstract*-Deadtime is a critical design target for soft switching dc/dc converters. On the one hand, the deadtime is necessary to ensure safety operation of the devices in one switching leg; on the other hand, enough deadtime is required to achieve zero voltage switching (ZVS) operation. Due to the complexity of LLC converters, traditionally, the deadtime selection is either based on engineering experience or inaccurate analysis of converter, which leads to an unoptimized deadtime. Specifically, a large deadtime will lead to the efficiency degradation due to the body diode conduction during deadtime. The ZVS operation cannot be completely achieved with a small deadtime, which will also degrade the converter efficiency. Therefore, there is a demand for the accurate analysis of deadtime effect on LLC converters. In this paper, an accurate and in-depth analysis of deadtime effect on LLC converter is performed with the aid of time domain analysis. But the proposed adaptive deadtime strategies can also be implemented based on the experiment or simulation results for those who do not have access to time domain analysis of LLC converters. Based on the analysis, novel adaptive deadtime strategies are proposed for LLC converter. Compared with traditional fixed deadtime strategy, around 1% efficiency improvement is achieved for a 125 W experimental prototype during the whole operating range.**

I. Introduction

With the ever-increasing demand on power converter efficiency, especially under light load operation conditions, converter optimizations are of great interest to improve the system efficiency performance. Commonly, lots of efforts have been put to optimize the converter circuit parameters. For example, in [1], a computer-aided automated design algorithm is developed to find the optimized circuit parameters.

Manuscript received September 14, 2020; revised December 15, 2020, and January 05, 2021; accepted January 29, 2021. This work was supported by Shaanxi Provincial Key Laboratory of Industrial Automation under Grant SLGPT2019KF01-14. (*Corresponding Author: Yuqi Wei and Quanming Luo*)

Yuqi Wei was with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, Chongqing University, Chongqing, China, and now he is with the the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA. (E-mail: yuqiwei@uark.edu)

Quanming Luo is with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, China, and is with School of Electrical Engineering, Shaanxi University of Technology. (E-mail: lqm394@126.com)

Zhiqing Wang was with the Department of Electrical Engineering, Chongqing University, Chongqing, China and she is now with monolithic power systems, Chengdu, China (E-mail: 569810311@qq.com).

H. Alan Mantooth is with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA. (E-mail: mantooth@uark.edu)

However, the dead time analysis is ignored and only optimization on the circuit parameters is presented. In [2], the LLC converter is optimized at the peak gain operating point, although the voltage gain performance of the converter can be fully explored. The converter is operating at the boundary of zero voltage switching (ZVS) operation and zero current switching (ZCS) operation. In addition, the deadtime design and analysis are missed. In [3], the deadtime is selected as the converter specifications, so it is known for engineers beforehand. In [4], a complete step by step design optimization algorithm is proposed for LLC converter. However, the deadtime optimization is not performed. Therefore, it can be concluded that most of the LLC converter design algorithms either ignore deadtime effect or treat it as known parameter.

However, deadtime is important for LLC converter performance. Deadtime can directly affect the soft switching performance of the switches, which is critical in today's very high frequency applications, where dv/dt or electro-magnetic interference (EMI) are critical issues in applications with wide band gap (WBG) devices [5, 6]. A large deadtime will lead to efficiency degradation caused by the conduction loss of body diode, and a small deadtime will lead to incomplete of ZVS operation, and ultimately cause high EMI noise and even destruction of power converters. Thus, optimization on LLC converter deadtime can improve both converter efficiency and EMI performances. In [7], the complete analysis of ZVS operation of LLC converter is performed. The necessary condition for ZVS operation is that there should be a negative current before the switch is turning on. The sufficient condition is that the deadtime is large enough to charge/discharge the parasitic capacitances. The author analyzed that an extreme large deadtime will lead to the loss of ZVS operation, which are commonly ignored in existing literature. Nevertheless, the analysis is performed based on the inaccurate frequency domain analysis. In addition, only the analysis is presented, while the design and optimization of deadtime are missed. There are some references focus on the ZVS performance analysis of unregulated LLC converters or DC transformers (DCX), where the converter is operating at resonant frequency operating point [8, 9]. However, in most applications, the LLC converters are operating in a wide switching frequency range to satisfy the converter voltage gain requirement. In these applications, the analysis at resonant frequency point is no longer true. In [10], the ZVS analysis for full-bridge LLC converter is presented. It is found out that the real ZVS requirement for full-bridge LLC converter is $L_m < t_{dead}/(8 \times C_{oss} \times f_r)$ instead of traditional

requirement $L_m<t_{dead}/(16\times C_{oss}\times f_r)$. Thus, a large magnetizing inductance value can be selected, which reduces the circulating current and conduction losses, ultimately improves converter efficiency. However, the deadtime analysis is still based on frequency domain and the derived ZVS requirement is only valid at resonant frequency point.

In [11], the minimum deadtime is optimized to satisfy the ZVS operation requirement under the worst operating case. For LLC converter, it is tricky to achieve ZVS operation at maximum input voltage and minimum output power. The required maximum switching frequency and minimum deadtime are optimized to improve converter efficiency. Again, inaccurate frequency domain analysis is used, which leads to unsatisfactory results.

In addition, in most of the existing literature in academia, the deadtime is fixed during whole operating range. By selecting the deadtime based on the worst operating case, the efficiency degradation and even ZVS lost under other circuit conditions may occur. From industry point of view, the commercial resonant mode controllers, like NCP1399 series from ON Semiconductor [12], UCC256303 LLC resonant controller from Texas Instrument [13], L6699 resonant controller from STMicroelectronics [14], adaptive deadtime strategies are all adopted to improve the converter efficiency during the whole operation range. The general idea for these adaptive deadtime strategies is to use a dv/dt detector to recognize the realization of ZVS operation, and then turned on the primary switch. Although the optimized deadtime can be generated during the whole operation range, the high switching frequency characteristic of power converters makes the dv/dt detection circuit sensitive to circuit noises and parasitics, which reduces the power converter reliability in high power applications.

To fully optimize the converter performance and improve reliability during whole operation conditions, novel adaptive deadtime strategies are proposed in this paper. Firstly, the deadtime analysis for LLC converter is implemented with accurate time domain analysis. Then, based on the analysis results, the adaptive deadtime strategies are proposed. Finally, experiment results are presented to validate the effectiveness of the proposed strategy. In addition, efficiency comparisons between the proposed strategies and traditional strategy are made. Discussions are made to summarize the application scenarios and considerations for the proposed adaptive deadtime strategies.

II. Deadtime Analysis for LLC Converter with Time Domain Analysis

The asymmetric half-bridge LLC converter shown in Fig. 1 is used to demonstrate the ZVS operation mechanism. Please note that similar analysis and method can be used for other LLC topologies as discussed in [15]. In Fig. 1, C_{ossp1} and C_{ossp2} are the output capacitance of primary switch, C_W is the transformer wiring capacitance, C_{osss1} and C_{osss2} are the secondary rectifier diodes output capacitance.

During the deadtime, the necessary condition to achieve ZVS operation can be expressed as Eq. (1) [7]. The detailed analysis on the secondary parasitic capacitance influence on primary switch ZVS performance can be found in [8].

$$Q = i_{off}\times t_{dead} \ge 2\cdot C_{ossp}\cdot V_i + C_{stray}\cdot V_i + C_W\cdot V_i + \frac{1}{N}\cdot C_{osss}\cdot 2V_o \quad (1)$$

where i_{off} is the primary switch turn-off current, which can be viewed constant during deadtime since the deadtime is very short, and t_{dead} is the deadtime.

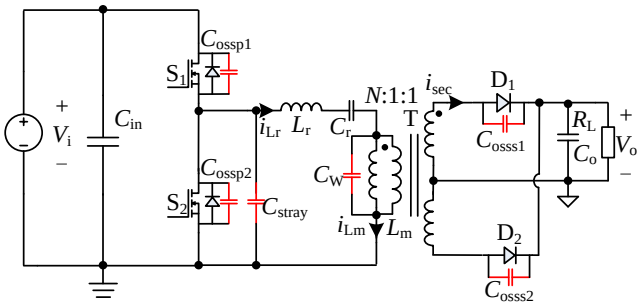


Fig. 1. Asymmetric half-bridge LLC converter with parasitic capacitances.

From Eq. (1), to satisfy the deadtime requirement, the information of primary switch turn-off current is required. Traditionally, the analysis is performed based on first harmonic analysis (FHA), which assumes that the converter is operating at resonant frequency point. Then, the primary switch turn-off current can be simply derived as

$$i_{off} = \frac{NV_o}{4L_m f_r} \quad (2)$$

By substituting Eq. (2) into Eq. (1), a design criteria for the deadtime or magnetizing inductance value is derived.

However, Eq. (2) is no longer true when the converter is not operating at the resonant frequency point, which will lead to miscalculation of the required deadtime. Many LLC papers are using Eq. (2) to either design deadtime or magnetizing inductance value. For example, in [16], the magnetizing inductance value is designed as

$$L_m = \frac{t_{dead}}{8C_{ossp}f_r} \quad (3)$$

In Eq. (3), the other circuit parasitic capacitances are not considered, which will lead to a larger magnetizing inductance value than the real magnetizing inductance value to satisfy the ZVS operation. With a large magnetizing inductance value, the ZVS operation condition may not be satisfied.

In [17], the ZVS analysis is performed under no load operation, and the magnetizing inductance value is selected based on the no load ZVS requirement. Clearly, although the ZVS operation can be achieved during the whole operating range, a large deadtime or small magnetizing inductance value should be selected, which degrades the converter efficiency performance under heavy and medium load operation conditions.

Generally, in the existing publications, the deadtime or magnetizing inductance value is either designed based on the resonant frequency operating point or no load operating point. The first design method will result in insufficient ZVS operation under light load operation in above resonant frequency region. The second design method will result in

excessive deadtime for medium and heavy load operation conditions. Thus, there is a demand for adaptive deadtime strategy that can adjust the converter deadtime based on the circuit operating conditions.

The commercial resonant mode controllers utilize dv/dt detector to recognize the ZVS realization of switch, and generate the corresponding gating signal. However, with the ever increasing demand for high frequency operation and the penetration of wide band gap devices, the switch dv/dt is very large, which challenges the dv/dt detector design. In addition, due to the small signal characteristic of dv/dt, it is sensitive to circuit noise, which affects the reliable operation of the converter.

In this paper, the adaptive deadtime strategies are proposed based on the large signals, which resolves the issue of sensitive to circuit noises of commercial resonant mode controllers. To obtain the accurate desired deadtime under different circuit conditions, the time domain analysis method is utilized.

A. Introduction of the Developed Time Domain Analysis Based Evaluation Tool

The issue with FHA analysis method is that when the LLC resonant converter is not operating at resonant frequency point, the calculated switch turn-off current based on FHA is different from the actual turn-off current. Fig. 2 makes comparisons between the theoretical results and simulation results for the LLC resonant converter when load resistance equals 5 Ω and 50 Ω with different input voltage. For the conventional FHA based analysis method, the switch turn-off current is independent of the converter input voltage and output power. However, when compared with the accurate time domain analysis (TDA) results, it can be seen that except at resonant frequency operation, where the FHA analysis results are close to the actual results, in other operation regions, considerable errors between the theoretical results and actual results exist, which will make the ZVS analysis inaccurate. In addition, the ZVS operation may not be ensured in the whole operation range since the converter is designed simply at resonant frequency point for FHA method.

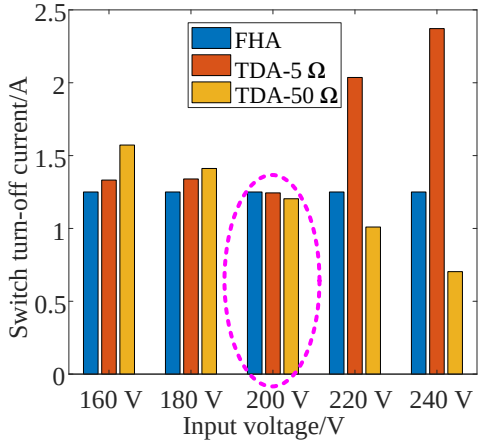


Fig. 2. Switch turn-off current comparison between conventional FHA and accurate TDA.

Therefore, the motivation of using time domain analysis in this paper is to improve the analysis accuracy, which can help optimize the LLC resonant converter. Since time domain analysis is not the novelty of this paper, many papers have discussed the time domain analysis process for the LLC resonant converter [1, 17], only the general principles regarding the time domain analysis are discussed in this paper. In addition, brief introductions will be made on the developed time domain analysis based evaluation tool.

Firstly, the general principles for the time domain analysis for LLC resonant converter are discussed.

Step 1: Operation stages of LLC resonant converter

There exist three operation stages for LLC resonant converter, namely, P, O, and N stage, the equivalent circuits are shown in Fig. 3. When the voltage across the magnetizing inductor is clamped by the positive output voltage NV_o, the converter is operating in P stage; if the magnetizing inductor is clamped by the negative output voltage $-NV_o$, the converter is operating in N stage; during the O stage operation, the magnetizing inductor is not clamped by the output voltage.

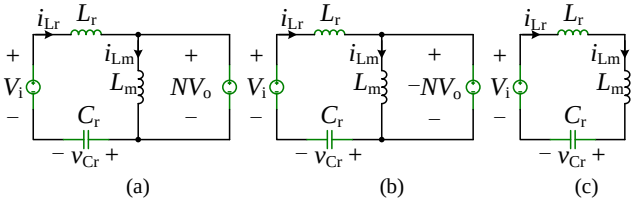


Fig. 3. Three operation stages for LLC resonant converter. (a) P stage; (b) N stage; (c) O stage.

The circuit equations for each operation stage can be derived based on the Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL).

Step 2: Non-linear equations

For an LLC resonant converter, there are many different operation modes based on the sequence of the operation stages in half of the switching cycle [1, 17]. For example, the PO operation mode means that the LLC resonant converter is operating at P operation stage first and then followed by an O operation stage. The following principles are used to derive the non-linear equations: 1) continuity of circuit voltages and currents: at the stage transition point, the circuit voltages and currents should be same by using equations from two operation stages; 2) symmetric characteristic of circuit voltages and currents: the voltage or current value at initial of the switching cycle and the value at the end of the half switching cycle are symmetric; 3) power conservation law: assuming there is no loss for the converter so that the input power equals output power. Based on these characteristics, the non-linear equations can be derived. By using the mathematical software, the circuit solutions can be derived. The details of these non-linear equations can be found in Appendix.

Step 3: Switch turn-off current

Once the circuit is solved in *Step 2*, the switch turn-off current can be easily calculated, which can be used to perform the ZVS analysis for LLC resonant converter.

Step 4: Calculating the optimized deadtime

Based on the circuit parameters and parasitic capacitors, the required minimum deadtime can be found by satisfying the inequality (1).

With the aid of the time domain model and the calculation mechanism discussed above, a ZVS analysis evaluation tool for LLC resonant converters is developed based on the MATLAB graphical user interface (GUI). Brief introductions are made for the developed evaluation tool. Fig. 4 shows the overall structure of the developed evaluation tool. It mainly includes the following seven parts: 1) topology structure selection: according to [15], for LLC resonant converter, there are mainly five structures for the primary inverter and three structure for the secondary rectifier. Then, based on the different combinations of inverter and rectifier, there are mainly 15 different LLC topologies that can be selected based on the converter specifications. Generally speaking, stacked structure is favored in high input voltage applications; full-bridge structure is preferred in high power applications; half-bridge structures are advantageous in low power and step-down applications. For the secondary rectifier, the full-bridge rectifier is preferred in high output voltage applications; the transformer center-tapped rectifier is advantageous in high output current applications due to the reduction of conduction loss; the voltage doubler rectifier is usually adopted in step-up applications. The developed evaluation tool includes all 15 different LLC topologies, which is convenient in real applications; 2) circuit parameters: similar to commercial simulation software, the circuit parameters are required as input; 3) closed-loop selection: there are typically three closed-loop strategies, namely, constant output voltage, constant output current, and constant output power. The users can select the output regulation type based on the converter specifications and applications; 4) circuit parasitic capacitors: for the ZVS analysis of LLC resonant converters, the parasitic capacitors are required. The primary switch and secondary rectifier junction capacitances are modelled as a function of the device voltage stress.

$$C_{oss} = k_4 \cdot e^{k_3 V_{DS}} + k_2 \cdot e^{k_1 V_{DS}} \tag{4}$$

where k_1-k_4 are the coefficients of the equation, which can be obtained by using curve fitting tool. In this research, the data is extracted from the manufacture datasheet, the "cftool" in the MATLAB is used to get k_1-k_4. The curve fitting results are presented in the Appendix.

In most of the design, the junction capacitances of the primary switch and secondary rectifier are regarded as constant values at the input voltage and output voltage level, respectively. However, from the ZVS waveform, during the transition, the voltage across the primary switch is varying from input voltage to zero, correspondingly, the junction capacitor of the primary switch should be a variable based on the C-V curve provided by the manufacture. Therefore, instead of a constant junction capacitance value, an equivalent junction capacitance should be used to perform the ZVS analysis and design [24]. The equivalent junction capacitance for the primary switch and secondary rectifier can be calculated as

$$C_{eq} = \frac{\int_0^{V_i or V_O} C_{oss}(v)dv}{V_i or V_o} \tag{5}$$

5) calculate and run buttons: by clicking the "Calculate" button, the ZVS analysis will start running and results will be shown; by clicking the "Refresh" button, the results will be removed; 6) analysis results: after running the analysis, the important results are demonstrated, including the required switching frequency, switch turn-off current, calculation time, and required deadtime; 7) current waveform: the resonant inductor current and magnetizing inductor current waveforms are plotted.

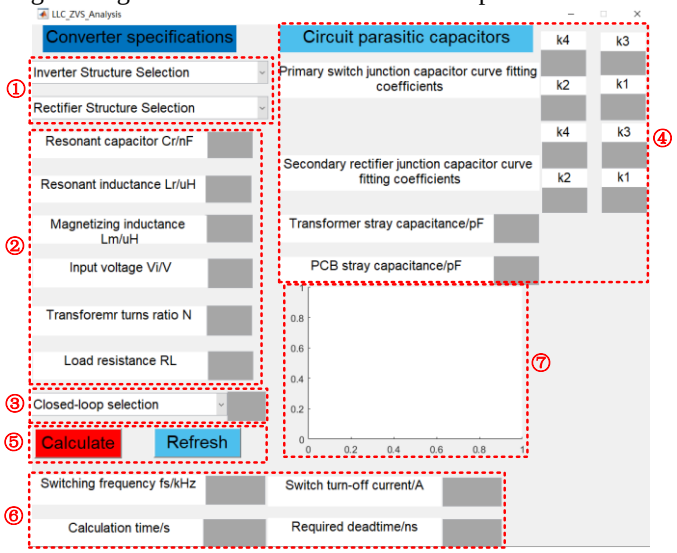


Fig. 4. Overall structure of the developed ZVS evaluation tool for LLC resonant converters.

Fig. 5 shows a specific analysis result of the evaluation tool. It can be seen that the calculation time is very short (less than 0.5 seconds) when you compared with commercial simulation software. A live demonstration is provided in the supplementary files to show the operation of the developed evaluation tool. In addition, it is very convenient to perform iterations with the aid of the developed evaluation tool by adding "for" loops in the code. Therefore, for the proposed adaptive deadtime strategy, the required data for the curve fitting or look-up tables can be easily generated.

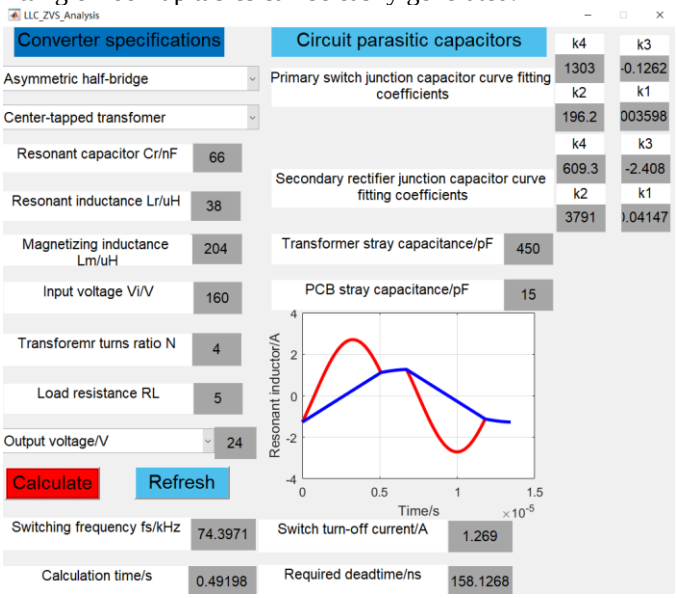


Fig. 5. ZVS analysis result for a specific LLC resonant converter.

B) ZVS Analysis for LLC Resonant Converter in Different Operation Regions

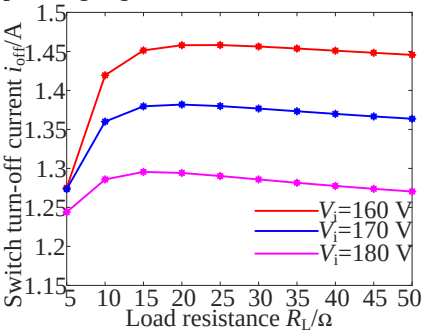
With the aid of the developed evaluation tool, the ZVS analysis for LLC resonant converter in different operation regions is made. The circuit parameters optimization is not the focus of this paper, which are treated as known parameters. The main focus of this paper is the deadtime optimization. The converter specifications are summarized in Table 1.

TABLE. I. CONVERTER SPECIFICATIONS

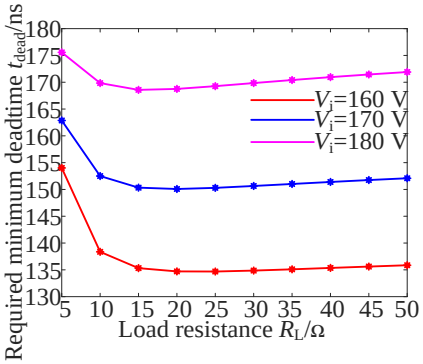
Description	Value
Input voltage V_i	160 V-240 V
Output voltage V_o	24 V
Output power P_o	11.5 W-115 W
Resonant frequency f_r	100 kHz
Resonant capacitor C_r	66 nF
Resonant inductor L_r	38 μH
Magnetizing inductor L_m	204 μH
Transformer turns ratio N	4
Primary switch	C3M0075120K
Secondary rectifier diode	IPB026N06N
Transformer wiring capacitance C_W	450 pF
Printed circuit board (PCB) stray capacitance C_{stray}	15 pF

1). Below Resonant Frequency Operation Region

When the input voltage is below 200 V, the LLC converter is operating in below resonant frequency region. Fig. 6(a) shows the turn-off current with different input voltage and output power. Clearly, the switch turn-off current increases with the decrease of output power initially, which makes the ZVS operation easier to be achieved under low output power applications. When the load further decreases, the switch turn-off current slightly decreases too. On the other hand, with the increase of input voltage, the switch turn-off current is decreasing. Thus, the worst case to achieve ZVS operation in below resonant frequency region is at rated output power. Fig. 6(b) shows the required minimum deadtime with different circuit conditions. The maximum deadtime around 175 ns is required at the rated output power. Overall, in below resonant frequency operating region, the deadtime variation is small.



(a) Primary switch turn-off current

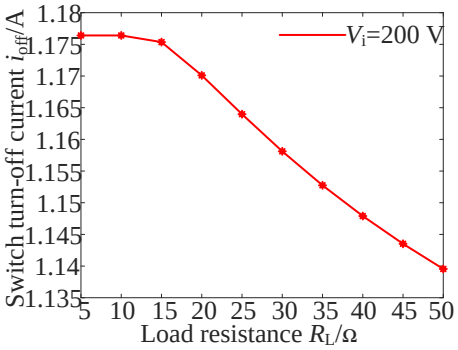


(b) Required minimum deadtime

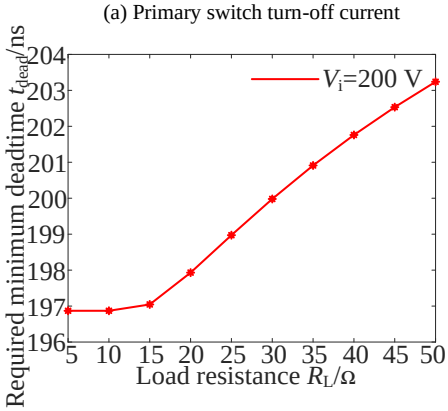
Fig. 6. ZVS analysis in below resonant frequency region.

2). At Resonant Frequency Point Operation

At resonant frequency operating point, the primary switch turn-off current and required minimum deadtime are shown in Fig. 7. The primary switch turn-off current does not vary with the output power at resonant frequency operating point since the first two digits are same. This results also explain why the traditional analysis method only valid for resonant frequency operating point. At this operating point, the magnetizing inductor is always clamped by the output voltage, so Eq. (2) can be used to calculate the turn-off current. While in other situations, turn-off current cannot be calculated by using Eq. (2).



(a) Primary switch turn-off current



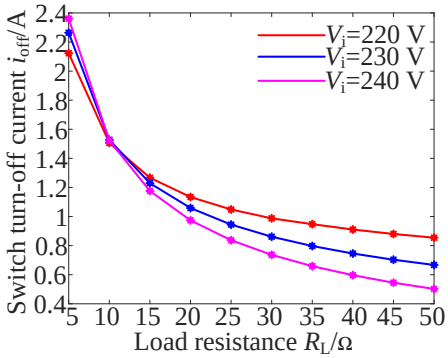
(b) Required minimum deadtime

Fig. 7. ZVS analysis at resonant frequency point.

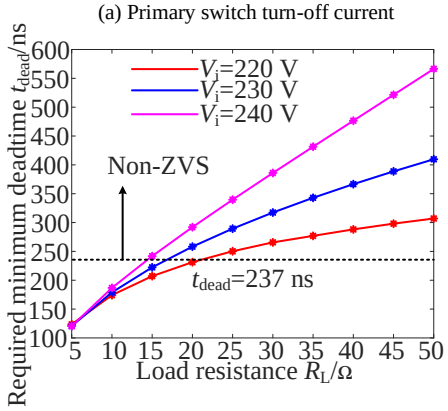
3). Above Resonant Frequency Operation Region

Fig. 8 shows the switch turn-off current and required minimum dead time with different input voltage and output power in above resonant frequency region. Clearly, the switch

turn-off current decreases with the output power, so a large deadtime is necessary under light load operation. As shown in Fig. 8(b), the maximum required deadtime is around 570 ns. Based on the above analysis, it can be concluded that the worst case for ZVS operation occurs when input voltage reaches its maximum value and the output power reaches its minimum value.



(a) Primary switch turn-off current



(b) Required minimum deadtime

Fig. 8. ZVS analysis in above resonant frequency region.

The conclusions for the ZVS analysis based on the specific LLC resonant converter can also be applied for other LLC converters with different circuit parameters. ZVS analysis is performed for the LLC converter proposed in [23] and the results are shown in the Appendix, which have the same conclusions in this Section. The reasons for these conclusions can be expressed as follows: 1) in below resonant frequency region, the converter is operating in PO or OPO operation mode, then, the switch turn-off current is determined by the O operation stage, where the magnetizing inductor is resonating with resonant inductor and resonant capacitor. Under heavy load condition, the voltage across the magnetizing inductor is small and even negative due to the large voltage drop on the other elements, so the slop for magnetizing inductor current is either very small or negative, which makes the primary switch turn-off current small. In contrast, under light load conditions, the voltage across the magnetizing inductor is large, so the current slope is large, which results in a large switch turn-off current. Therefore, the worst case operation is usually achieved at the minimum input voltage with rated output power in below resonant frequency region; 2) at resonant frequency operation, the voltage across the magnetizing inductor can be assumed to be clamped by the output voltage during the whole operation range. Therefore, there would be no difference on the magnetizing inductor current; 3) in above resonant frequency region, the higher the output power, the larger the resonant inductor current, the switch turn-of current is around the maximum inductor current. Therefore, it is easier to achieve ZVS operation under heavy load conditions when compared with light load conditions.

III. Proposed Adaptive Deadtime Strategies

Traditionally, the deadtime is selected based on Eqs. (1) and (2). With the given parameters in table 1, the required deadtime is calculated as t_{dead}=237 ns. Although the ZVS operation can be ensured at resonant frequency point and below resonant frequency region, the ZVS operation is lost at above resonant frequency region with medium and light load operation as labeled in Fig. 8(b), which will cause efficiency degradation and EMI issues, especially under light load conditions. Moreover, hard switching operation will also lead to circuit noise, which affects the reliability and safety operation of the converter. Therefore, the traditional deadtime strategy is not preferred in applications require above resonant frequency operation. On the other hand, if the deadtime is selected based on the worst case, like 570 ns in this case, then, the deadtime is more than five times greater than that under the minimum input voltage and maximum output power operation condition. Therefore, adaptive deadtime strategy is required to increase converter efficiency and improve converter performance.

Inspired by Fig. 6-Fig. 8, clearly, the required deadtime is different with both input voltage and output power. Then, two adaptive deadtime strategies can be proposed: 1) adaptive deadtime strategy based on input voltage; 2) adaptive deadtime strategies based on input voltage and output power.

A. Adaptive Deadtime Strategy based on Input Voltage

Firstly, the deadtime is adjusted based on the input voltage, which is normally given for the LLC converters for the purpose of protection, so there is no additional requirement on the converter hardware. To satisfy the ZVS operation during the whole output power range, the maximum deadtimes at specific input voltage level are used and drawn in Fig. 9. The proposed adaptive deadtime strategy can be simply achieved by using a look-up table. Clearly, by using the proposed adaptive deadtime strategy, the LLC converter efficiency performance can be optimized during the whole operating range. The detailed control diagram is shown in Fig. 10. The control signal v_c is generated from the proportional integral (PI) controller. Then, after the voltage-controlled oscillator (VCO) block, the required switching frequency f_s can be generated to regulate the output voltage.

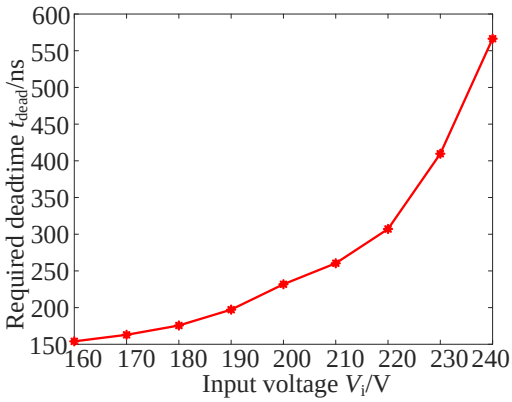


Fig. 9. Relationship between input voltage and required deadtime.

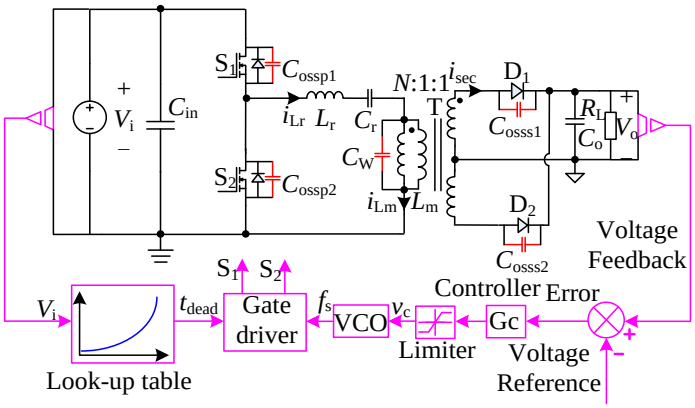


Fig. 10. Control diagram of the proposed adaptive deadtime strategy based on input voltage.

B. Adaptive Deadtime Strategy based on Input Voltage and Output Power

Although the adaptive deadtime strategy based on input voltage can optimize the converter performance to some extent, as shown in Fig. 8, the required deadtime varies with output power or load greatly in above resonant frequency operation region. For example, at 240 V, the required deadtime at minimum output power is more than five times larger than that at heavy load. Thus, a simple adaptive deadtime strategy based on input voltage is not enough, the influence of output power should also be taken into consideration.

Traditionally, to detect the output power, the output current is required. However, the current measurement equipment is bulky and lossy, especially at high output current applications. Although some chip based current transformers are commercially available, the cost and complexity of the system are increased. Thus, there is a need for a simple but effective method to recognize the output power of the converter. Fortunately, with the aid of time domain analysis, the relationship between the output power or load resistance and other variables can be explored, which can indirectly reflect the output power. Theoretically, the parameters for LLC converter including: 1) input voltage V_i; 2) output voltage V_o; 3) resonant inductor L_r; 4) resonant capacitor C_r; 5) magnetizing inductor L_m; 6) transformer turns ratio N; 7) load resistance R_L; 8) switching frequency f_s. For these eight parameters, by giving any seven of them, the last one can be mathematically derived by using time domain analysis. Therefore, in the real application, the circuit parameters are known, the input voltage and output voltage are sampled, the switching frequency is generated based on the closed-loop controller. Therefore, only the load resistance value is unknown. Thus, the switching frequency generated by the closed-loop controller can actually reflect the output power.

Next, the relationship between the switching frequency and load resistance is investigated under different input voltage. As shown in Fig. 6-Fig. 8, the deadtime variation with load resistance is small when the converter is operating at resonant frequency or below resonant frequency. Thus, to reduce the control complexity, the load resistance influence is only investigated in above resonant frequency operation region. Fig. 11 shows the relationship between the normalized switching frequency and load resistance value for LLC converter operating in above resonant frequency region. Based on Fig. 11, the load resistance value can be estimated based on the input voltage and switching frequency.

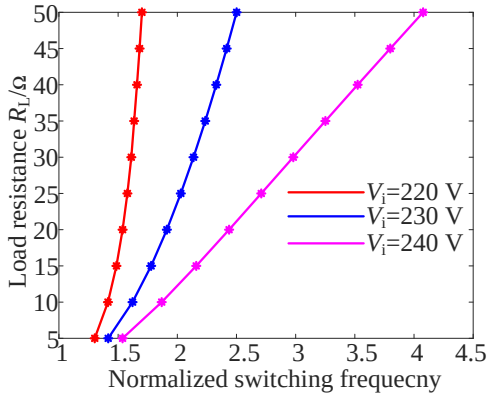


Fig. 11. Relationship between the normalized switching frequency and load resistance value.

Therefore, for the adaptive deadtime strategy that considers both input voltage and output power, the control diagram in Fig. 10 can be modified as shown in Fig. 12. Both the input voltage and switching frequency are required to determine the optimized deadtime under different circuit conditions.

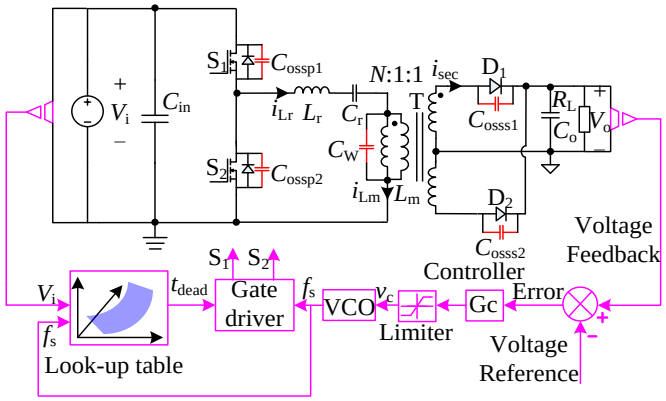


Fig. 12. Control diagram of the proposed adaptive deadtime strategy based on input voltage and output power.

The implementation flow chart for the proposed adaptive deadtime strategies can be summarized as shown in Fig. 13, where V_{ref} is the desired output voltage and ΔV_o is the accepted output voltage variation. In the case discussed in this paper, V_{ref}=24 V, and ΔV_o=1 V. The details about each step are shown below.

Step 1: Input circuit parameters and parasitics to the developed deadtime evaluation tool

In this step, the circuit components parameters and corresponding parasitics are set in the developed deadtime evaluation tool. The main purpose of this step is to generate the required data for curve fitting or look-up tables based on the selected adaptive deadtime strategy.

Step 2: Select adaptive deadtime strategy

As analyzed in this paper, there are two adaptive deadtime strategies, one is solely based on the input voltage, while another one is based on both the input voltage and output power. It is recommended that the input voltage based adaptive deadtime strategy can be used when the converter output power variations are small. Otherwise, to further optimize the converter performance, the input voltage and output power based adaptive deadtime strategy is preferred.

Step 3: Generate and load the look-up tables

Based on the system requirement, the input voltage and/or the output power variation step can be determined. Then, with the aid of the developed evaluation tool, the look-up tables can be generated easily. Finally, the look-up tables are loaded in the digital controller.

Step 4: Sampling input voltage V_i and output voltage V_o

The input voltage and output voltage are required during the whole operation range to achieve the adaptive deadtime control and output voltage closed-loop control.

Step 5: Large and fixed deadtime

Initially, a large and fixed deadtime is applied for the LLC converter to ensure ZVS operation during the non-steady state conditions, like start up, load change, and input voltage change etc. The non-steady state conditions are determined based on the output voltage, if the detected output voltage is not at the proximity of the reference value, then, the converter is considered to work in non-steady state conditions.

Step 6: Frequency control to regulate output voltage

During the operation, the frequency control is enabled to regulate the converter output voltage.

Step 7: Record switching frequency f_s

The switching frequency is only recorded when the converter reaches into steady state operations, where the output voltage is at the proximity of the reference value. Then, the recorded switching frequency is combined with the input voltage to obtain the output power information.

Step 8: Look-up tables and Optimized deadtime

In this step, the required input voltage and switching frequency information are send to the look-up tables to generate the optimized deadtime based on the selected adaptive deadtime strategy. Then, the converter is operating with the optimized deadtime to improve the performance.

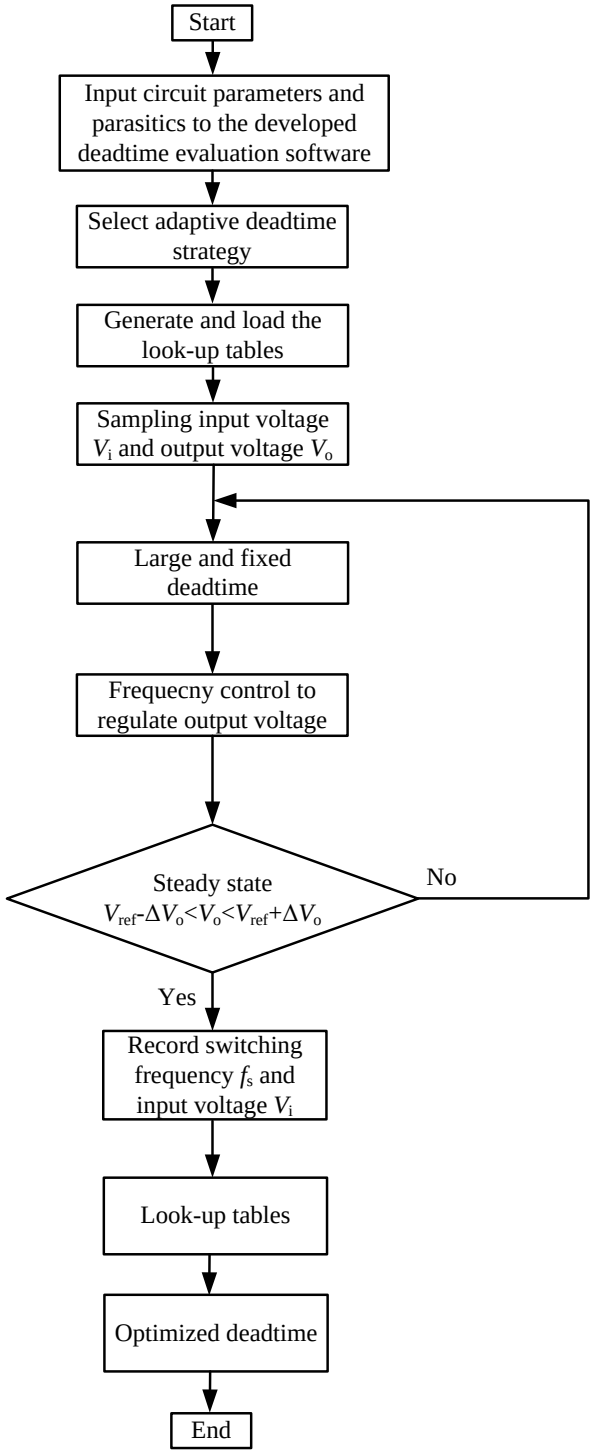


Fig. 13. Flow chart of the proposed adaptive deadtime strategy in real circuit implementation.

Therefore, when the transients occur, the converter will operate in non-steady state conditions. According to the flow chart, once the converter output voltage is not at the proximity of the reference voltage, the adaptive deadtime strategy is disabled and the converter is operating with a large and fixed deadtime. Thanks to the large deadtime during transients, the ZVS operation can also be ensured during the transients, which

avoids device failures caused by over-temperature and over-stress.

As can be seen from Fig. 13, the proposed adaptive deadtime generate the optimized deadtime based on the large signal input voltage and switching frequency. It is understandable that these signals have higher noise immunity when compared with the d*v*/d*t* signal that required in commercial resonant mode controllers.

IV. Experiment Results

In this Section, experiment results are presented to validate the effectiveness of the proposed strategy, and efficiency comparisons between the proposed adaptive deadtime strategies and traditional deadtime strategy are made. Fig. 14 shows the picture of the experimental setup.

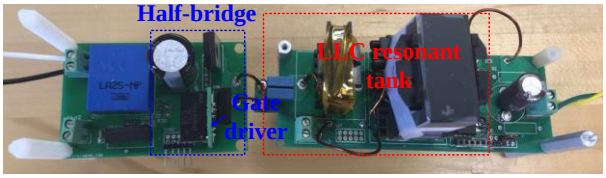
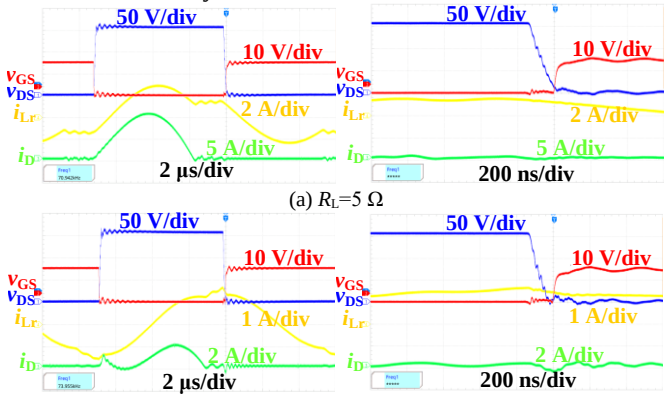


Fig. 14. Picture of the experiment setup.

A. Steady-State Experiment Waveforms

Fig. 15 shows experiment waveforms with the proposed adaptive deadtime strategy based on input voltage when input voltage equals 160 V, where v_{GS} is the gate voltage of S_2, v_{DS} is the voltage across S_2, i_{Lr} is the resonant inductor current, and i_D is the secondary rectifier diode current. The deadtime is 160 ns when input voltage equals 160 V. Clearly, the ZVS operation is achieved for primary switch during whole power range. More importantly, the ZVS operation is easier to be achieved under light load operation as shown in Fig. 15(b), which agrees with the theoretical analysis.

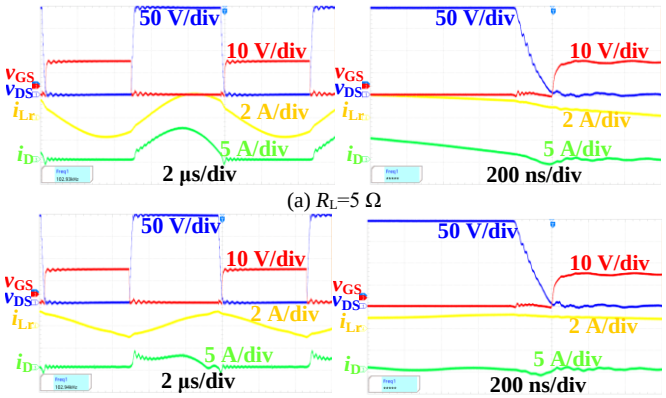


(a) R_L=5 Ω

(b) R_L=50 Ω

Fig. 15. Experiment waveform in below resonant frequency region.

Fig. 16 shows the experiment waveforms at resonant frequency point. The required deadtime is around 210 ns. As analyzed previously, the ZVS operation at resonant frequency with different output power are almost same.

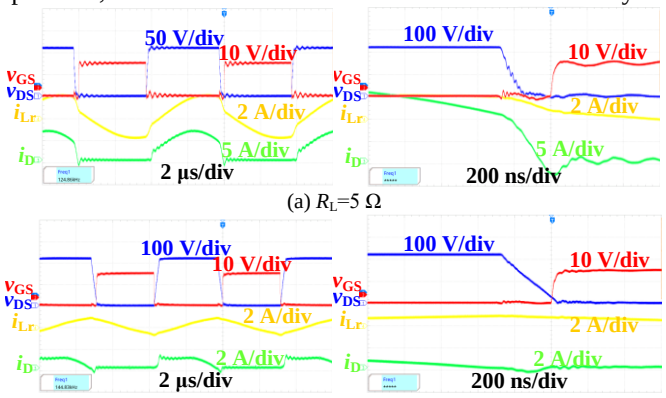


(a) R_L=5 Ω

(b) R_L=50 Ω

Fig. 16. Experiment waveform at resonant frequency point.

Fig. 17 shows the experiment waveform in above resonant frequency region when input voltage equals 220 V. The required deadtime is 310 ns. Clearly, under heavy load, the ZVS operation is much easier to be achieved than the light load operation, the results in consistent with the theoretical analysis.

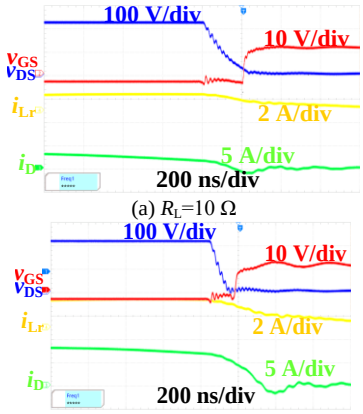


(a) R_L=5 Ω

(b) R_L=50 Ω

Fig. 17. Experiment waveform in above resonant frequency region with adaptive deadtime strategy based on input voltage.

From Fig. 15 to Fig. 17, it can be seen that with the proposed adaptive deadtime strategy based on input voltage, it can optimize the converter deadtime in below resonant frequency region as we analyzed. However, in above resonant frequency operating region, the required deadtime under heavy load is much smaller than that under light load. Thus, the efficiency under heavy load operation is degraded due to the conduction loss of body diode. To further increase the converter efficiency, the adaptive deadtime strategy based on both input voltage and output power is adopted. Fig. 18 shows the corresponding experiment waveforms with different load resistance. Clearly, under heavy load operation, the required deadtime is much smaller than that of the light load operation. Thus, by introducing the effect of output power in the proposed adaptive deadtime strategy, the converter operation performance can be further improved.

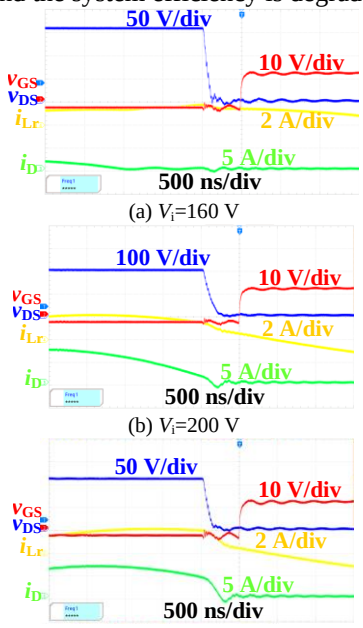


(a) R_L=10 Ω

(b) R_L=5 Ω

Fig. 18. Experiment waveform in above resonant frequency region with adaptive deadtime strategy based on both input voltage and output power.

To make comparisons, the traditional fixed deadtime strategy is utilized. To ensure the ZVS operation during the whole operating range, a deadtime of 570 ns is required. Fig. 19 shows some ZVS experiment waveform with deadtime of 570 ns when R_L=5 Ω. Clearly, the deadtime is too large for other operating conditions expect the worst case operating point, the body diode will conduct and the system efficiency is degraded.



(a) V_i=160 V

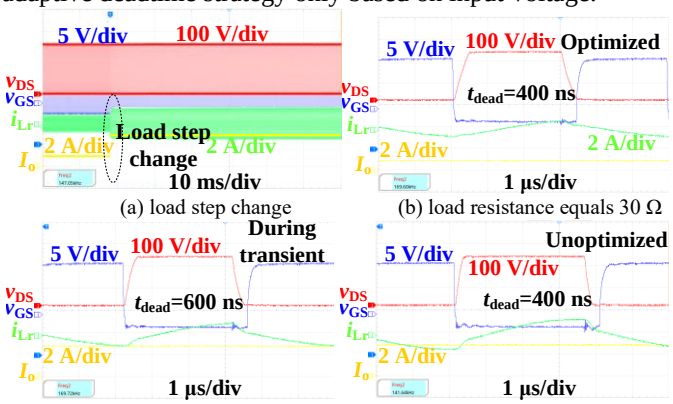
(b) V_i=200 V

(c) V_i=220 V

Fig. 19. Experiment waveform with fixed deadtime strategy.

B. Transient Operation Experiment Waveforms

To validate the effectiveness of the proposed adaptive deadtime strategy during transient operations, the corresponding experiment results are presented and analyzed. Fig. 20 shows the experiment waveforms when the load changes from 30 Ω to 8 Ω with the input voltage based adaptive deadtime strategy, where the converter input voltage is fixed at 220 V. When the converter is operating under light load, the deadtime is optimized. Once the load step change occurs, the converter will operate in non-steady state condition, where a large and fixed deadtime of 600 ns is generated to ensure the ZVS operation. When the new steady state operation is reached, the adaptive deadtime is enabled and since only the input voltage is used to generate the optimized deadtime, the same deadtime that used in light load condition is generated for the new steady state condition as shown in Fig. 20(d). Clearly, the deadtime is not optimized for heavy load conditions with the adaptive deadtime strategy only based on input voltage.



(a) load step change

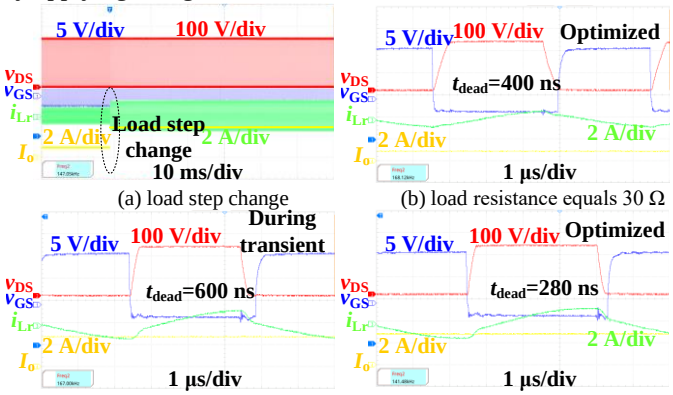
(b) load resistance equals 30 Ω

(c) during transient operation

(d) load resistance equals 8 Ω

Fig. 20. Dynamic experiment waveform when there is a load step change with input voltage based adaptive deadtime strategy.

Therefore, to further improve the converter performance, the switching frequency is also used to generate the optimized deadtime. It is understandable that under light load conditions, a higher switching frequency is required when compared with heavy load conditions. Thus, by introducing the switching frequency into the look-up table, the deadtime can be optimized by taking both input voltage and output power into considerations. Fig. 21 shows the experiment waveforms under the same condition with input voltage and output power based adaptive deadtime strategy. Clearly, the deadtime is optimized both in light load and heavy load conditions. Meanwhile, the ZVS operation is also ensured during the transient operations by applying a large and fixed deadtime.



(a) load step change

(b) load resistance equals 30 Ω

(c) during transient operation

(d) load resistance equals 8 Ω

Fig. 21. Dynamic experiment waveform when there is a load step change with input voltage and output power based adaptive deadtime strategy.

Clearly, for the input voltage based adaptive deadtime strategy, the deadtime is constant under light load and heavy load conditions, which is 400 ns. On the other hand, the deadtime generated based on both input voltage and output power is 400 ns under light load condition and only 280 ns

under heavy load condition. An optimized deadtime is generated and the body diode conduction during deadtime can be further reduced.

Videos are also attached in the supplementary files to demonstrate the dynamic operations of the proposed adaptive deadtime strategies. In **Video 1**, it shows the operation of the input voltage based adaptive deadtime strategy with light load operation (R_L=50 Ω), **Video 2** shows the heavy load operation (R_L=5 Ω). It can be seen that different optimized deadtime is generate based on the input voltage. For light load operation, the deadtime is optimized, while for the heavy load operation, the deadtime is unoptimized. In **Video 3**, it shows the operation of the input voltage based adaptive deadtime strategy when there is a load step change. Although the input voltage based adaptive deadtime strategy can optimize the converter deadtime to some extent, when the output power changes, especially for the heavy load operation, the converter deadtime is not optimized. Thus, in **Video 4,** it shows the operation of the input voltage and output power based adaptive deadtime strategy, it can be seen that the optimized deadtime can be generated under different load conditions.

C. Efficiency Comparison

Fig. 22 shows the efficiency comparison between the proposed strategy and the traditional fixed deadtime strategy. Clearly, with the proposed adaptive deadtime strategy, around 1% efficiency improvement can be achieved. In above resonant frequency region, the adaptive deadtime strategy with both input voltage and output power has better efficiency performance that the adaptive deadtime strategy only with input voltage.

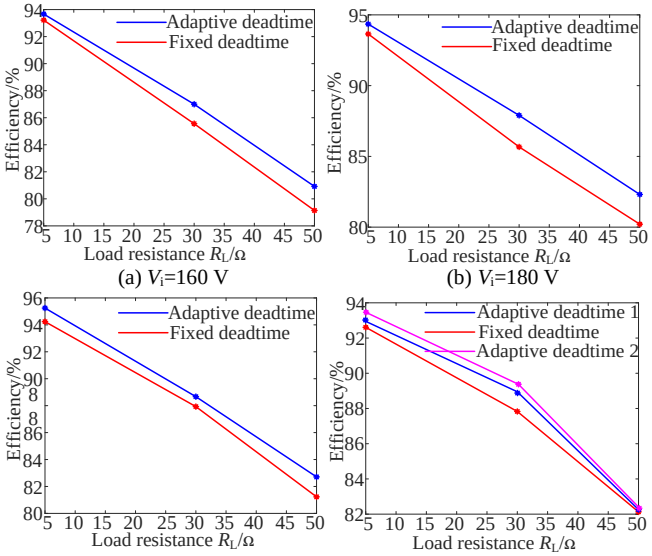


Fig. 22. Efficiency comparison under different operating conditions.

D. Discussions and Contributions

This paper discusses the analysis, design, and implementation of two adaptive deadtime strategies to improve the LLC converter performance. The recommendations for each adaptive deadtime strategy in real applications are summarized as follows:

1) Based on the analysis results, it can be concluded that the deadtime variation with output power is small in below resonant frequency region. Therefore, to reduce control complexity, the adaptive deadtime strategy based on input voltage can be used for LLC converters that are designing only in below resonant frequency operation region, like the LLC converters in [17, 18].

2) In above resonant frequency operation region, the required deadtime variation with output power is significant. Thus, the adaptive deadtime strategy based on both input voltage and output power can be adopted for LLC converters include above resonant frequency operation, like the LLC converters in [19, 20].

3) Since the deadtime variation is very small at resonant frequency operation, the simple fixed deadtime strategy can be adopted for LLC converters that are designing at resonant frequency operation, which are also known as DC transformers (DCT) [21, 22].

The contributions of this paper can be summarized in the following aspects:

1) An accurate ZVS analysis method for LLC resonant converters is proposed. Conventionally, the ZVS analysis is performed by using the first harmonic approximation (FHA) method and assuming a constant junction capacitor for the primary switch, which results in considerable errors. To improve the accuracy, this article proposed to use time domain analysis and equivalent junction capacitance to analyze and design the LLC resonant converters, which has higher accuracy.

2) The proposed adaptive deadtime strategy can improve the LLC converter performance. Traditionally, the fixed deadtime strategy is applied for the LLC converter. If the fixed deadtime is selected based on the nominal operating point, in some operation regions, the ZVS operation cannot be achieved, which degrades the converter efficiency and generate considerable EMI noise. On the other hand, if the fixed deadtime is selected based on the worst case operation, in some operation regions, the deadtime is not optimized since deadtime is too large, and the body diode conduction loss during deadtime will degrade the converter efficiency. With the aid of the proposed adaptive deadtime strategy, the deadtime can be optimized during the whole operation range.

3) Compared with the adaptive deadtime strategy used in commercial LLC controllers, the proposed adaptive deadtime strategy has the advantages of simple, no cost, and high noise immunity and reliability. Only the input voltage is sampled for the proposed adaptive deadtime strategies, which is commonly available for the engineers for the purpose of protection. The output power is indirectly reflected by the switching frequency and input voltage, which requires no additional sampling circuit. In addition, input voltage and switching frequency are large signals, which has higher noise immunity when compared with the dv/dt signal required in the commercial controllers.

4) An evaluation tool is developed, which can simplify the application of the proposed adaptive deadtime strategy. The required look-up tables or data can be easily generated. In addition, the developed evaluation tool is suitable for all LLC topologies with different circuit parameters. For those who do not have access to time domain analysis of LLC converters,

experiment or simulation data can be used to implement the proposed adaptive deadtime strategies based on the system requirements.

5) Although the proposed adaptive deadtime strategies are implemented based on a specific converter, the methods and conclusions in this article can be applied for any LLC converters with different devices and circuit parameters. For example, the following conclusions we have drawn from the analysis are also true for other LLC converters with different circuit parameters: 1) in below resonant frequency operation region, the required deadtime variation with output power is small; 2) at resonant frequency operating point, the required deadtime almost remain constant with different output power; 3) in above resonant frequency operation region, the required deadtime varies a lot with output power, and the most tricky operating point to satisfy ZVS operation is at the maximum input voltage with minimum output power.

V. Conclusion

It was found out that the required deadtime for LLC converter varies with circuit operating conditions, especially in above resonant frequency region. To optimize converter performance, two adaptive deadtime strategies based on input voltage and output power are proposed. For LLC converters only operating in below resonant frequency operation region, the adaptive deadtime based on input voltage can be adopted. For the LLC converters including above resonant frequency operation region, the adaptive deadtime strategy based on input voltage and output power can be adopted. For the proposed adaptive deadtime strategies, the following features are achieved: 1) simple and no cost, this paper simply utilize the input voltage and switching frequency to achieve adaptive deadtime strategies; 2) the proposed strategies can be utilized for all LLC topologies; 3) ZVS operation during the whole operating range is ensured; 4) efficiency improvement is achieved when compared with traditional strategies.

Appendix

A. Time domain modelling for LLC converter

Before we talk about the derivation, some definitions of the LLC resonant converter are summarized in Table A1. The main purpose of Table A1 is to simplify the expressions of equations.

Table A1. LLC CONVERTER DEFINITIONS

Angular series resonant frequency ω_r	$\omega_r = \frac{1}{\sqrt{L_r C_r}}$
Angular parallel resonant frequency ω_m	$\omega_m = \frac{1}{\sqrt{(L_r+L_m)C_r}}$
Operation angle θ	$\theta = \omega_r t$
Normalized switching frequency F	$F = \frac{\omega_s}{\omega_r}$
Half period switching cycle γ	$\gamma = \frac{\omega_r}{2 f_s}$
Converter voltage gain m	$m = \frac{nV_o}{V_i}$
Normalized voltage V_{base}	$V_{base} = nV_o$
Normalized impedance Z_{base}	$Z_{base} = \sqrt{\frac{L_r}{C_r}}$
Normalized current I_{base}	$I_{base} = \frac{V_{base}}{Z_{base}}$
Normalized resonant capacitor voltage $m_{Cr}(\theta)$	$m_{Cr}(\theta) = \frac{V_{Cr}(\frac{\theta}{\omega_r})}{V_{base}}$
Normalized magnetizing inductor voltage $m_{Lm}(\theta)$	$m_{Lm}(\theta) = \frac{V_{Lm}(\frac{\theta}{\omega_r})}{V_{base}}$
Normalized resonant inductor voltage $m_{Lr}(\theta)$	$m_{Lr}(\theta) = \frac{V_{Lr}(\frac{\theta}{\omega_r})}{V_{base}}$
Normalized resonant inductor current $j_{Lr}(\theta)$	$j_{Lr}(\theta) = \frac{i_{Lr}(\frac{\theta}{\omega_r})}{I_{base}}$
Normalized magnetizing inductor current $j_{Lm}(\theta)$	$j_{Lm}(\theta) = \frac{i_{Lm}(\frac{\theta}{\omega_r})}{I_{base}}$
Normalized output current j_{out}	$j_{out} = \frac{i_{out}}{I_{base}}$
Normalized output load resistance r_L	$r_L = \frac{N^2 R_L}{Z_{base}}$
Inductor ratio λ	$\lambda = \frac{L_r}{L_m}$
Ratio of two resonant frequencies k_1	$k_1 = \frac{\omega_m}{\omega_r}$

Generally, there are three possible resonant stages during half period as shown in Fig. 3, which are denoted as P, O and N, respectively. The half switching period is denoted as γ, and the end of the first stage is denoted as α, while the end of the second stage is denoted as β. Take PO operation mode for an example, as shown in Fig. A1, the end of the fist P stage is α, and the end of second O stage is γ, which is half of the switching period. For those operation modes with three operation stages, like OPO or PON operation mode, anther angle β exists. Then, based on the normalization of the resonant unit, different resonant stages can be described mathematically as follows.

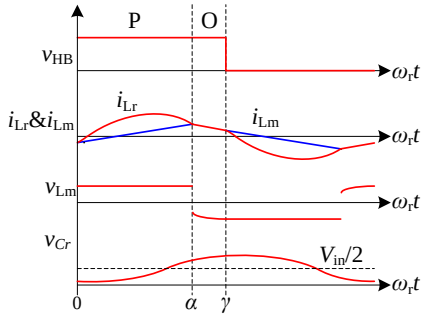


Fig. A1. Typical operation waveform for PO operation mode.

For P stage, the circuit can be solved as:

$$\begin{aligned} j_{\mathrm{LrP}}(\theta) &= j_{\mathrm{Lr}}(\theta_{ini})\cdot\cos(\theta-\theta_{ini}) \\ &\quad +[1/m-1-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\sin(\theta-\theta_{ini}) \\ j_{\mathrm{LmP}}(\theta) &= j_{\mathrm{Lm}}(\theta_{ini})+\lambda\cdot(\theta-\theta_{ini}) \\ m_{\mathrm{LmP}}(\theta) &= 1 \\ m_{\mathrm{CrP}}(\theta) &= 1/m-1-[1/m-1-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\cos(\theta-\theta_{ini}) \\ &\quad + j_{\mathrm{Lr}}(\theta_{ini})\cdot\sin(\theta-\theta_{ini}) \end{aligned} \tag{A1}$$

For N stage, the circuit can be solved as:

$$\begin{aligned} j_{\mathrm{LrN}}(\theta) &= j_{\mathrm{Lr}}(\theta_{ini})\cdot\cos(\theta-\theta_{ini}) \\ &\quad +[1/m+1-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\sin(\theta-\theta_{ini}) \\ j_{\mathrm{LmN}}(\theta) &= j_{\mathrm{Lm}}(\theta_{ini})-\lambda\cdot(\theta-\theta_{ini}) \\ m_{\mathrm{LmN}}(\theta) &= -1 \\ m_{\mathrm{CrN}}(\theta) &= 1/m+1-[1/m+1-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\cos(\theta-\theta_{ini}) \\ &\quad + j_{\mathrm{Lr}}(\theta_{ini})\cdot\sin(\theta-\theta_{ini}) \end{aligned} \tag{A2}$$

For O stage, the circuit can be solved as:

$$\begin{aligned} j_{\mathrm{LrO}}(\theta) &= j_{\mathrm{Lr}}(\theta_{ini})\cdot\cos[k_1\cdot(\theta-\theta_{ini})] \\ &\quad +k_1\cdot[1/m-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\sin[k_1\cdot(\theta-\theta_{ini})] \\ j_{\mathrm{LmO}}(\theta) &= j_{\mathrm{Lm}}(\theta) \\ m_{\mathrm{LmO}}(\theta) &= [-m_{\mathrm{CrO}}(\theta_{ini})+1/\mathrm{m}]/(1+\lambda) \\ m_{\mathrm{CrO}}(\theta) &= 1/m-[1/m-m_{\mathrm{Cr}}(\theta_{ini})]\cdot\cos[k_1\cdot(\theta-\theta_{ini})] \\ &\quad + j_{\mathrm{Lr}}(\theta_{ini})/k_1\cdot\sin[k_1\cdot(\theta-\theta_{ini})] \end{aligned} \tag{A3}$$

In this article, the PO operation mode is selected as an example. Based on the general principles discussed in Step 2 of Section II, the required non-linear equations for PO operation mode can be derived as follows.

$$\begin{cases} j_{\mathrm{Lr}}(0)-j_{\mathrm{Lm}}(0)=0 \\ j_{\mathrm{Lr}}(\alpha)-j_{\mathrm{Lm}}(\alpha)=0 \\ m_{\mathrm{Cr}}(0)+m_{\mathrm{Cr}}(\gamma)-\dfrac{1}{m}=0 \\ j_{\mathrm{Lr}}(0)+j_{\mathrm{Lr}}(\gamma)=0 \\ j_{out}r_L-1=0 \end{cases} \tag{A4}$$

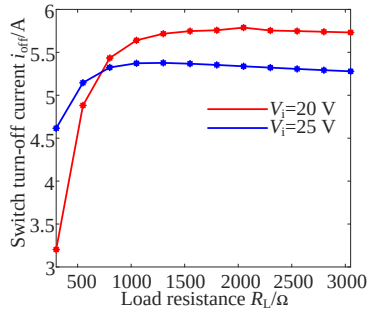
It is noted that θ_{ini} represents the initial angle of the stage, and the initial value of the resonant capacitor voltage, resonant inductor current and magnetizing inductor current can be described as $j_{\mathrm{Lr}}(0)$, $j_{\mathrm{Lm}}(0)$ and $m_{\mathrm{Cr}}(0)$, respectively. Finally, with the aid of mathematical software, the LLC converter in PO operation mode can be solved. In this article, the 'fslove' function in MATLAB is used to solve non-linear equations. The modelling process for other operation modes are same.

B. Curve fitting results for primary switch and secondary rectifier diode output capacitances

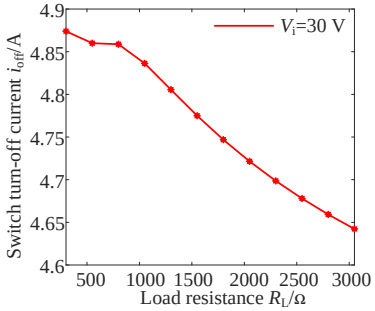
By extracting data from the datasheet provided by manufacture and using the curve fitting tool "cftool" in MATLAB, the coefficients in equation (4) for the semiconductor junction capacitance can be derived. The primary switch is selected as an example, and Fig. A2 shows the curve fitting results.

C. ZVS analysis for other LLC converter with different circuit parameters

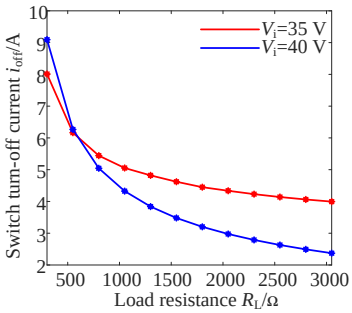
To validate the conclusions that we have drawn in Section II, the circuit parameters in [23] are used to analyze the switch turn-off current. Please note that the converter structure is also different, in [23], it is a full-bridge LLC resonant converter. The circuit parameters are: C_r=330 nF, L_r=3.9 μH, L_m=11 μH, N=1/7, $P_{o,max}$=150 W, V_o=210 V. Fig. A3 shows the switch turn-off current in different operation regions with different output power. Similarly, the following conclusions can be drawn: 1) in below resonant frequency region, the worst case occurs at rated output power. However, it is hard to say that the worst case in whole below resonant frequency region occurs at the minimum input voltage with rated output power or maximum input voltage with rated output power. As can be seen from Fig. A3(a), before the crossing point of two curves, the worst operation point is at the minimum input voltage with rated output power, while if the converter output power is lower than the crossing point corresponded output power, then, the worst operation point is not at the minimum input voltage. Nevertheless, most of the case, the worst operation point for below resonant frequency region occurs at the minimum input voltage with rated output power; 2) at resonant frequency operation, the switch turn-off current is almost independent of output power, so the ZVS operation at this point is almost same for different output power; 3) in above resonant frequency region, the worst case occurs at the maximum input voltage with the minimum output power and the primary switch turn-off current decreases dramatically with the decrease of output power.



(a) below resonant frequency region



(b) at resonant frequency operation



(c) above resonant frequency region

Fig. A3. Primary switch turn-off current in different operation regions with the circuit parameters in [23].

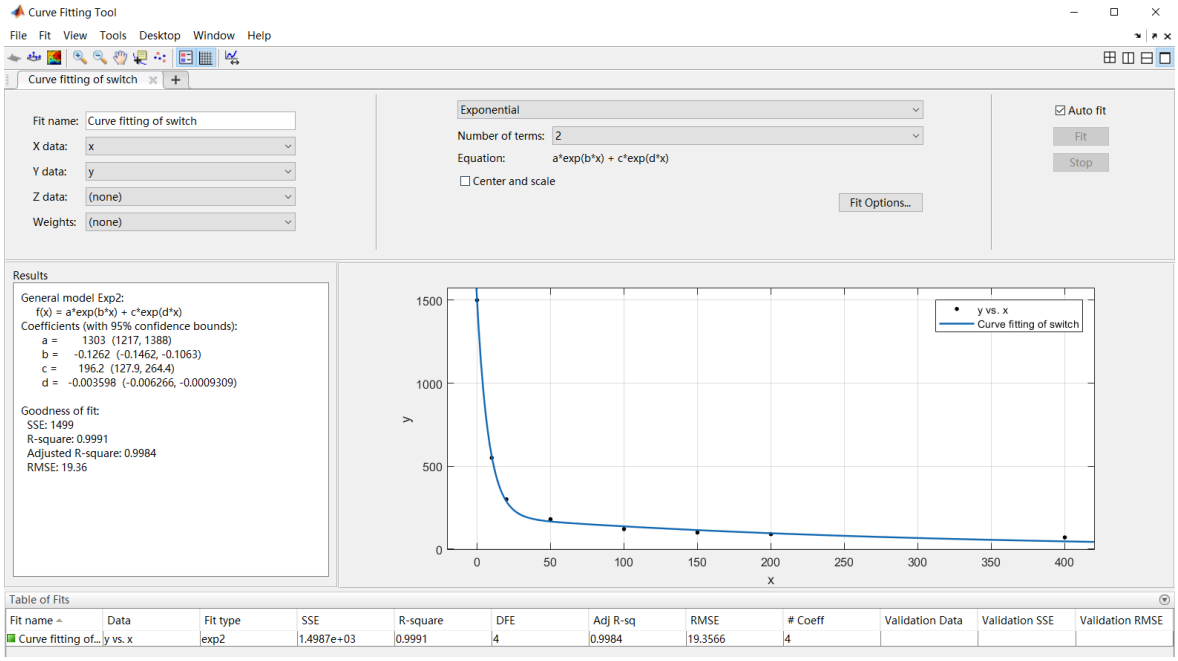


Fig. A2. Curve fitting result for primary switch with part number of C3M0075120K.

REFERENCES

[1] R. Yu, *et al*. "Computer-Aided Design and Optimization of High-Efficiency LLC Series Resonant Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3243-3256, Jul. 2012.

[2] X. Fang, H. Hu, Z. J. Shen and I. Batarseh, "Operation Mode Analysis and Peak Gain Approximation of the LLC Resonant Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985-1995, Apr. 2012.

[3] S. De Simone, C. Adragna, C. Spini and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006, pp. 200-207.

[4] Y. Wei, Q. Luo, Z. Wang and H. A. Mantooth, "A Complete Step by Step Optimal Design for LLC Resonant Converter," IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2020.3015094.

[5] S. Zhao, X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth, "A Review on Switching Slew Rate Control for Silicon Carbide Devices using Active Gate Drivers," IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.3008344.

[6] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao and H. A. Mantooth, "An Intelligent Versatile Model-Based Trajectory-Optimized Active Gate Driver for Silicon Carbide Devices," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 429-441, Mar. 2020.

[7] R. Ren, B. Liu, E. A. Jones, F. Wang, Z. Zhang and D. Costinett, "Accurate ZVS boundary in high switching frequency LLC converter," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

[8] W. Qin, L. Zhang and X. Wu, "Re-examination of ZVS Condition for MHz LLC Converter Operating at Resonant Frequency," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, 2018, pp. 1-4.

[9] H. Chen and X. Wu, "Analysis on the influence of the secondary parasitic capacitance to ZVS transient in LLC resonant converter," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 4755-4760.

[10] U. Kundu, K. Yenduri and P. Sensarma, "Accurate ZVS Analysis for Magnetic Design and Efficiency Improvement of Full-Bridge LLC Resonant Converter,' *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1703-1706, Mar. 2017.

[11] R. Beiranvand, B. Rashidian, M. R. Zolghadri and S. M. H. Alavi, "Optimizing the Normalized Dead-Time and Maximum Switching Frequency of a Wide-Adjustable-Range LLC Resonant Converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462-472, Feb. 2011.

[12] ON semiconductor, "NCP1399/D Current Mode Resonant Controller, with Integrated High-Voltage Drivers, High Performance", Rev. 17, Oct. 2019.

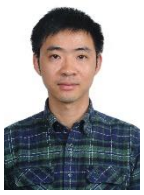
[13] Texas Instrument, "UCC256303 LLC Resonant Controller Enabling Ultra-Low Standby Power", Jan. 2019.

[14] STMicroelectronics, "L6699 Enhanced high voltage resonant controller", Jan. 2013.

[15] Y. Wei, Q. Luo and A. Mantooth, "Overview of Modulation Strategies for LLC Resonant Converter," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10423-10443, Oct. 2020.
[16] H. Wu, T. Mu, X. Gao and Y. Xing, "A Secondary-Side Phase-Shift-Controlled LLC Resonant Converter With Reduced Conduction Loss at Normal Operation for Hold-Up Time Compensation Application," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5352-5357, Oct. 2015.
[17] Y. Wei, Q. Luo, X. Du, N. Altin, J. M. Alonso and H. A. Mantooth, "Analysis and Design of the LLC Resonant Converter With Variable Inductor Control Based on Time-Domain Analysis," *IEEE Ind. Power Electron.*, vol. 67, no. 7, pp. 5432-5443, Jul. 2020.
[18] J. Deng, C. C. Mi, R. Ma and S. Li, "Design of LLC Resonant Converters Based on Operation-Mode Analysis for Level Two PHEV Battery Chargers," IEEE/ASME Transactions on Mechatronics, vol. 20, no. 4, pp. 1595-1606, Aug. 2015.
[19] M. M. Jovanović and B. T. Irving, "On-the-Fly Topology-Morphing Control—Efficiency Optimization Method for LLC Resonant Converters Operating in Wide Input- and/or Output-Voltage Range," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2596-2608, Mar. 2016.
[20] Z. Fang, T. Cai, S. Duan and C. Chen, "Optimal Design Methodology for LLC Resonant Converter in Battery Charging Applications Based on Time-Weighted Average Efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5469-5483, Oct. 2015.
[21] F. Liu, G. Zhou, X. Ruan, S. Ji, Q. Zhao and X. Zhang, "An Input-Series-Output-Parallel Converter System Exhibiting Natural Input-Voltage Sharing and Output-Current Sharing," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1166-1177, Feb. 2021.
[22] J. Lee, Y. Jeong and B. Han, "An Isolated DC/DC Converter Using High-Frequency Unregulated LLC Resonant Converter for Fuel Cell Applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2926-2934, Jul. 2011.
[23] X. Fang, H. Hu, Z. J. Shen and I. Batarseh, "Operation Mode Analysis and Peak Gain Approximation of the LLC Resonant Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985-1995, Apr. 2012.
[24] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063-8067, Dec. 2016.

Yuqi Wei (S'18) was born in Henan, China, in 1995. He received his B.S. degree in Electrical Engineering from Yanshan University, Hebei, China, in 2016, and his M.S. degree in Electrical Engineering from University of Wisconsin-Milwaukee (UWM), Wisconsin, U.S.A., in 2018. He received another M.S. degree in Electrical Engineering from Chongqing University, Chongqing, China, in 2019. He is currently working toward the Ph.D. degree at the University of Arkansas, Arkansas, U.S.A.

His current research interests include topology, modelling and control of DC/DC power converters and power factor correction AC/DC converters, wide band gap devices, active gate driving, and cryogenic power electronics.



Quanming Luo (M'14) was born in Chongqing, China, in 1976. He received his B.S., M.S., and Ph.D. in Electrical Engineering from Chongqing University, in 1999, 2002, and 2008, respectively. He was with the Emerson Network Power Co. Ltd., Shenzhen, China, as a Research and Development Engineer from 2002 to 2005. Since 2005, he has been with the College of Electrical Engineering, Chongqing University, where he is currently a Professor. His current research interests include LED driving systems, communication power systems, power harmonic suppression, and power conversion systems in electrical vehicles.

Zhiqing Wang was born in Chongqing, China, in 1994. She received her B.S. degree and M.S. degree in Electrical Engineering from Chongqing University, Chongqing, China, in 2017 and 2020, respectively. Currently, she is working with monolithic power systems, Chengdu, China. Her current research interests include power converter topologies and advanced control for renewable energy systems.

H. Alan Mantooth (S'83 – M'90 – SM'97 – F'09) received the B.S. and M.S. degrees in electrical engineering from the University of Arkansas in 1985 and 1986, respectively, and the Ph.D. degree from the Georgia Institute of Technology in 1990. He then joined Analogy, a startup company in Oregon, where he focused on semiconductor device modeling and the research and development of modeling tools and techniques. In 1998, he joined the faculty of the Department of Electrical Engineering at the University of Arkansas, Fayetteville, where he currently holds the rank of Distinguished Professor. His research interests now include analog and mixed-signal IC design & CAD, semiconductor device modeling, power electronics, and power electronic packaging. Dr. Mantooth helped establish the National Center for Reliable Electric Power Transmission (NCREPT) at the UA in 2005. Professor Mantooth serves as the Executive Director for NCREPT as well as two of its centers of excellence: the NSF Industry/University Cooperative Research Center on GRid-connected Advanced Power Electronic Systems (GRAPES) and the Cybersecurity Center on Secure, Evolvable Energy Delivery Systems (SEEDS) funded by the U.S. Department of Energy. In 2015, he also helped to establish the UA's first NSF Engineering Research Center entitled Power Optimization for Electro-Thermal Systems (POETS) that focuses on high power density systems for transportation applications. Dr. Mantooth holds the 21st Century Research Leadership Chair in Engineering. He serves as Immediate Past-President for the IEEE Power Electronics Society in 2019-20 and the Editor-in-Chief of IEEE Open Journal of Power Electronics. Dr. Mantooth is a Fellow of IEEE, a member of Tau Beta Pi and Eta Kappa Nu, and registered professional engineer in Arkansas.